CLAIMS

1. An Integrated device in emitter switching configuration, said device being integrated in a chip of semiconductor material of a first conductivity type, said chip having a first surface and a second surface opposite to each other, said device comprising:

a first transistor having a base region, an emitter region and a collector region;

a second transistor having a not drivable terminal for collecting charges, which is connected with the emitter terminal of the first transistor;

a quenching element of the first transistor, which discharges current therefrom when said second transistor is turned off, said quenching element being coupled with the base terminal of the first transistor and with the other not drivable terminal of the second transistor, said quenching element having at least one Zener diode made in polysilicon, said at least one polysilicon Zener diode being formed on the second surface of said chip and comprising a polysilicon layer having at least one zone of the first conductivity type and at least one zone of a second conductivity type in order to form at least one P-N junction.

2. The Integrated device according to claim 1, wherein said chip comprises a first region of the second conductivity type which extends from the second surface into the chip and a second region of the first conductivity type which extends from the second surface into the first region, and the first region, the second region and a portion of the chip comprised between the first region and the first surface forming respectively the base region, the emitter region and the collector region of the first transistor.

3. Integrated device according to claim 2, wherein said first transistor and said second transistor are bipolar transistors and said chip comprises a third region of the second conductivity type which extends from the second surface into the second region and a fourth region of the first conductivity type which extends from the second surface into the third region, each of the second region, of the third region and of the fourth region forming respectively the collector region, the base region and the emitter region of the second transistor.

4. Integrated device according to claim 2, comprising a third bipolar transistor connected with the third transistor in a Darlington configuration wherein the emitter terminal of the first transistor is connected with the base terminal of the first transistor and the collector terminal of the first transistor is connected with the collector terminal of the third transistor.

5. Integrated device according to claim 2, wherein said second transistor is a MOS transistor and said chip comprises a couple of third regions of the second conductivity type which extend from the second surface into the second region and a couple of fourth regions of the first conductivity type which extend from the second surface into each one of third regions, each of the second region, of the third regions and of the fourth regions forming respectively the drain region, the body region and the source region of the second transistor.

6. Integrated device according to claim 1, wherein said first conductivity type of the semiconductor material is of N-type and said second conductivity type of semiconductor material is of P-type.

7. Integrated device according to claim 1, wherein said first conductivity type of the semiconductor material is of P-type and said second conductivity type of semiconductor material is of N-type.

8. Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises a polysilicon Zener diode the cathode of which is connected with the base terminal of the first transistor and the anode of which is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises only one P-N junction.

9. Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises first and second polysilicon Zener diodes in back to back

connection wherein the anode of the first Zener diode is connected with the anode of the second Zener diode and the cathode of the first Zener diode is connected with the base terminal of the first transistor and the cathode of the second Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises two P-N junctions.

10. Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises first and second polysilicon Zener diodes in back to back connection wherein the cathode of the first Zener diode is connected with the cathode of the second Zener diode and the anode of the first Zener diode is connected with the base terminal of the first transistor and the anode of the second Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises two P-N junctions.

11. Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises a series of couples of polysilicon Zener diodes in back to back connection wherein the cathode of the one Zener diode of one couple is connected with the cathode of the other Zener diode of the same couple and so on and the anode of the first Zener diode is connected with the base terminal of the first transistor and the anode of the last Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises a series of P-N junctions.

12. Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises a series of couples of polysilicon Zener diodes in back to back connection wherein the anode of the one Zener diode of one couple is connected with the anode of the other Zener diode of the same couple and so on and the cathode of the first Zener diode is connected with the base terminal of the first transistor and the cathode of the last Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises a series of P-N junctions.

13. Integrated device according to claim 1, wherein said at least one polysilicon Zener diode is formed on the second surface of the chip in a zone over an insulated layer.

14. Integrated device according to claim 1, comprising a diode the cathode of which is connected with the collector terminal of the first transistor and the anode of which is connected with said other not drivable terminal of the second transistor, said diode conducing when the voltage value at the collector terminal becomes lower than the voltage value at the other not drivable terminal of the second transistor.

15. Process for manufacturing an integrated device in emitter switching configuration in a substrate of a semiconductor material of a first conductivity type, comprising:

forming a first region of a second conductivity type inside the semiconductor material substrate, the first region comprising the base region of a first transistor and a region, allocated between the first region and a first surface of the substrate, forming the collector region of the first transistor;

forming a second region of the first conductivity type which extends into the first region, the second region comprising the emitter region of the first transistor;

forming a second transistor, said second transistor having a charge collection terminal formed by the second region;

forming at least one third region of the second conductivity type, which extends from a second surface of the substrate into the second region, said second surface being opposed to said first surface;

forming at least a fourth region of the first conductivity type in the third region;

forming conductive material over the second surface of the semiconductor material substrate;

forming a first insulated layer over the second surface of said semiconductor material substrate;

forming a polysilicon layer over a zone of said insulating layer;

doping said polysilicon layer with a first dopant of a conductivity type,

doping only some parts of said polysilicon layer with a second dopant with a conductivity opposite to that of the first dopant in order to form at least one polysilicon P-N junction;

placing a second insulating layer over said polysilicon layer;

partially removing said second insulating layer in order to form bores to contact said at least one polysilicon P-N junction and to contact the terminals of the integrated device on the semiconductor material;metalizing for filling up with metal said holes.

16. Process according to claim 15, wherein said at least one P-N junction comprises two P-N junctions.

17. Process according to claim 15, wherein said at least one P-N junction comprises only one P-N junction.

18. Process according to claim 15, wherein said at least one P-N junction comprises more than two P-N junctions.

19. Process according to claim 15, wherein said at least one third region of the second conductivity type is only one region of the second conductivity type and said at least one fourth region is only one region.

20. Process according to claim 15, wherein said at least one third region of the second conductivity type comprises at least one region and said at least one fourth region of the first conductivity type comprises two region couples, each one of said region couples of said fourth region being inside each region of the couple of said at least one third region.

21. Process according to claim 15, wherein said first conductivity type of the semiconductor material is of N-type and said second conductivity type of semiconductor material is of P-type.

22. Process according to claim 15, wherein said first conductivity type of the semiconductor material is of P-type and said second conductivity type of semiconductor material is of N-type.

23. A device, comprising:

a semiconductor substrate of a first type of conductivity;

a first region having a second type of conductivity formed in the semiconductor substrate;

a second region having the first type of conductivity formed over and in contact with the first region, the first and second regions and a portion of the substrate underlying the first region forming base, emitter and collector, respectively, of a first transistor;

a second transistor formed in the substrate and including a third region having the first type of conductivity, formed over and in contact with the second region;

the second transistor also including a fourth region having the second type of conductivity, formed in the third region;

an insulating layer selectively formed on an upper surface of the substrate;

a polysilicon layer selectively formed on the insulating layer; and

a zener diode formed in the polysilicon layer and including first and second junction regions having first and second types of conductivity, respectively, the diode being configured to discharge current from the first region when the second transistor is turned off.

24. The device of claim 23 wherein the second transistor is a bipolar transistor and further includes a fifth region having the first type of conductivity and formed in the fourth region, the third, fourth and fifth regions comprising collector, base and emitter, respectively, of the second transistor.

25. The device of claim 23 wherein the second transistor is a MOS transistor and further includes:

a fifth region having the second type of conductivity, formed in the third region and separated from the fourth region by a portion of the third region;

sixth and seventh regions having the first type of conductivity and formed in the fourth and fifth regions, respectively; and

a polysilicon region formed on the insulating layer, apart from the polysilicon layer and over the portion of the third region, the polysilicon region, the sixth and seventh regions, and the fourth region comprising gate, source and drain, respectively, of the MOS transistor.

26. The device of claim 23 wherein the zener diode is one of a plurality of zener diodes formed in the polysilicon layer, the plurality of diodes connected in series, and alternating in polarities.

27. A method, comprising:

forming, in a semiconductor substrate having a first type of conductivity, a first transistor by forming a region having a second type of conductivity and forming a second region over and in contact with the first region and having the first type of conductivity, wherein the first and second regions and a portion of the substrate below the first region are the base, emitter and collector, respectively, of the first transistor;

forming a second transistor in the substrate and over the first transistor, wherein the first and second transistors are in series configuration;

selectively forming an insulating layer over an upper surface of the substrate above the first and second transistors;

selectively forming a polysilicon layer over the insulating layer; and

forming a zener diode in the polysilicon layer, configured to drain current from the first transistor when the second transistor is turned off.

28. The method of claim 27, wherein the second transistor is a bipolar transistor.

29. The method of claim 27, wherein the second transistor is a MOS transistor.

30. The method of claim 27 wherein the zener diode is one of a plurality of diodes formed in the polysilicon layer.